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1 Workstations (panel discussion): a complete solution to the VLSI designer?

Prathima Agrawal, Frederick L. Cohen, Chet Palesko, Hung-Fai Stephen Law, Mark Miller, Mike Price, David W. Smith, Nicholas P. Van Brunt

June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**

Full text available: pdf(759.20 KB) Additional Information: full citation, abstract, index terms

The dynamics of today's electronics industry introduces enormous pressure on chip designers to come up with chip designs in a very limited time. This is due partly to the short life cycle of application specific products in the marketplace. The availability of powerful graphics processors and microprocessors with processing powers comparable to minicomputers has introduced several stand alone workstations into the design arena. Designer productivity is improved to a great extent by the prov ...

2 A practical one-semester "VLSI design" course for computer science (and other) majors

Robert A. Walker

March 1999 **ACM SIGCSE Bulletin , The proceedings of the thirtieth SIGCSE technical symposium on Computer science education**, Volume 31 Issue 1

Full text available: pdf(646.82 KB) Additional Information: full citation, abstract, references, index terms

This paper describes the development and content of a "VLSI Design" course. We had two main goals for the course: to develop a one-semester course for computer science (and other) majors, and to give the students practical experience with real industrial tools. To meet those goals, we provided only enough material on logic design and IC operation to orient the students, focused on FPLD-based design, and used high-quality design tools. We also found a wealth of free material available on the web, ...

3 Session 4A: Circuit structure in formal verification: Induction-based gate-level verification of multipliers

Ying Tsai Chang, Kwang Ting Tim Cheng

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(77.24 KB) Additional Information: full citation, abstract, references, citings, index terms

We propose a method based on unrolling the inductive definition of binary number multiplication to verify gate-level implementations of multipliers. The induction steps successively reduce the size of the multiplier under verification. Through induction, the

verification of an n-bit multiplier is decomposed into n equivalence checking problems. The resulting equivalence checking problems could be significantly sped up by simple structural analysis. This method could be generalized to the verific ...

4 The VHSIC hardware description language (VHDL) program
Al Dewey
June 1984 **Proceedings of the 21st conference on Design automation**

Full text available: pdf(196.27 KB) Additional Information: full citation, abstract, references, citings, index terms

The emergence of the importance of VLSI design automation and the VLSI custom/semicustom industry has spurred a wide-spread interest in hardware description languages. Starting in 1981, the VHSIC Program has acted as a catalyst to develop a standard hardware description language that could beneficially serve the government, industry, and academic communities. This panel will discuss from different viewpoints the issues associated with VLSI interoperability standards and the potential role o ...

5 Vex—A CAD toolbox
Jules P. Bergmann, Mark A. Horowitz
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(65.80 KB) Additional Information: full citation, references, citings, index terms

6 Cost and benefit models for logic and memory BIST
Juin-Ming Lu, Cheng-Wen Wu
January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(135.56 KB) Publisher Site Additional Information: full citation, references, index terms

7 Design technology productivity in the DSM era (invited talk)
Andrew B. Kahng
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Full text available: pdf(126.72 KB) Additional Information: full citation, abstract, references, index terms

Future requirements for design technology are always uncertain due to changes in process technology, system implementation platforms, and applications markets. To correctly identify the design technology need, and to deliver this technology at the right time, the design technology community - commercial vendors, captive CAD organizations, and academic researchers - must focus on improving design technology time-to-market and quality-of-result. Put another way, we must address the well-known ...

8 A strategy for real-time kernel support in application-specific HW/SW embedded architectures
Steven Vercauteren, Bill Lin, Hugo De Man
June 1996 **Proceedings of the 33rd annual conference on Design automation**

Full text available: pdf(91.67 KB) Additional Information: full citation, references, citings, index terms

9 System design tools for broadband telecom network applications
B. Lin

March 1996 **Proceedings of the 1996 European conference on Design and Test**

Full text available: pdf(612.66 KB) Publisher Site Additional Information: full citation, abstract

Outlines a design methodology for the design of hybrid software/hardware systems that are typically found in telecom network applications. This methodology is based on the results of an investigation and evaluation of an actual industrial system application for ATM (Asynchronous Transfer Mode) based broadband networks at Alcatel Bell. As a result of this investigation, we have developed a system design methodology based on a concurrent object-oriented programming model as the system behavioral s ...

Keywords: ATM, Alcatel Bell, C language, C++ models, Matisse, VHDL models, asynchronous transfer mode, broadband networks, broadband telecom network, concurrent object-oriented programming model, design flow, hardware description languages, object-oriented programming, system behavioral specification formalism, system design tools, system level model, system-level synthesis functionalities, telecommunication computing

10 Rational for and organization of the engineering information system program

A. J. Gadient, J. L. Ebel

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available: pdf(595.76 KB) Additional Information: full citation, abstract, references, index terms

The need for a robust, multi-user, integrated design environment for electronic systems is the result of the phenomenal growth in integrated circuit fabrication technology over the last decade. Attempts to develop "integrated" design environments highlight the current lack in design tool interoperability. The Very High Speed Integrated Circuits (VHSIC) program recognizes the importance of integrated design environments for the design of future defense electronic systems and for ...

11 Implementation of a SDH STM-N IC for B-ISDN using VHDL based synthesis tools

Juan Carlos Calderón, Enric Corominas, José M. Tapia, Luis París

September 1994 **Proceedings of the conference on European design automation**

Full text available: pdf(612.55 KB) Additional Information: full citation, references, index terms

12 ABLE: AMD backplane for layout engines

Kenneth W. Wan, Roshan A. Gidwani

July 1993 **Proceedings of the 30th international conference on Design automation**

Full text available: pdf(595.16 KB) Additional Information: full citation, references, index terms

13 An overview of VHDL language and technology

Moe Shahdad

July 1986 **Proceedings of the 23rd ACM/IEEE conference on Design automation**

Full text available: pdf(812.50 KB) Additional Information: full citation, abstract, references, citings, index terms

VHDL language and technology has been under development for the past five years, resulting in a hardware description language that enjoys widespread support within the industry. Version 7.2 of the language was released in August of 1985 and is being considered by the IEEE as a prime candidate for standardization. It is expected that a proposed standard based on Version 7.2 will be available in January of 1987. This standard will be accompanied by a VHDL Tutorial containing extensive example ...

14 An Introduction to IC Design under Linux

Toby Schaffer, Alan W. Glaser

July 1997 **Linux Journal**

Full text available: html(39.29 KB) Additional Information: full citation, abstract, references, index terms

Linux becomes a platform that can be used to create real world, working chips when freely available tools are used in concert

15 A system design methodology for software/hardware co-development of telecommunication network applications

Bill Lin

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Full text available: pdf(140.58 KB) Additional Information: full citation, references, citings, index terms

16 A conceptual framework for designing ASIC hardware

S. S. Leung, M. A. Shanblatt

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available: pdf(529.56 KB) Additional Information: full citation, abstract, references, index terms

A conceptual framework consisting of the design process, the design space, and the design repertoire for ASIC hardware is presented. An Inter-Level Design Process Model (ILDP) is proposed as a general model for expressing and implementing hierarchical design methodologies. The proposed conceptual framework is an effective instrument for bridging the increasingly wider gap between application engineers and VLSI designers.

17 Enhanced functionality by coupling the JESSI-COMMON-Framework with an ECAD framework

A. Kunzmann, R. Seepold

March 1995 **Proceedings of the 1995 European conference on Design and Test**

Full text available: pdf(732.76 KB) Publisher Site Additional Information: full citation, abstract

Within the electronic CAD domain there exist several frameworks each with a different set of services, which results in the specific support of dedicated design activities. One of the most innovative framework systems is the JESSI-COMMON-Framework (JCF). In contrast to JCF, a widespread ECAD framework (called FMCAD) has nearly complementary goals: while JCF offers strong support for working with consistent data concurrently, the basic functionality of FMCAD heavily supports the designer. In orde ...

Keywords: ECAD framework, FMCAD, JESSI-COMMON-framework, VLSI, circuit CAD, concurrent engineering, consistent data, dedicated design activities, electronic CAD domain, hybrid framework, integrated circuit design

18 Design-flow and synthesis for ASICs: a case study

Massimo Bombana, Patrizia Cavalloro, Salvatore Conigliaro, Roger B. Hughes, Gerry Musgrave, Giuseppe Zaza

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**

Full text available: pdf(111.78 KB) Additional Information: full citation, references, index terms

19 CAD and foundries for microsystems

J. M. Karam, B. Courtois, H. Boutamine, P. Drake, A. Poppe, V. Szekely, M. Rencz, K. Hofmann, M. Glesner

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(304.07 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

Besides foundry facilities, Computer-Aided Design (CAD)tools are also required to move microsystems from researchprototypes to an industrial market. Currently available CADtools need extensions before they can be used for theautomated design of micromachined devices.This paper presents a low cost access to microsystemtechnology (MST), applied by the CMP service, and based onthe use of existing microelectronics production lines, withadditional post-processing for microsystem specific 2D and3D str ...

20 TAE Plus: Transportable Applications Environment Plus: a user interface development environment

Martha R. Szczur, Sylvia B. Sheppard

January 1993 **ACM Transactions on Information Systems (TOIS)**, Volume 11 Issue 1

Full text available: pdf(1.99 MB)

Additional Information: full citation, abstract, references, citings, index terms

The Transportable Applications Environment Plus (TAE Plus) is a NASA-developed user interface development environment (UIDE) for the rapid prototyping, evaluation, implementation, and management of user interfaces. TAE Plus provides an intuitive What You See Is What You Get (WYSIWYG) WorkBench for designing an application's user interface. The WorkBench supports the creation and sequencing of displays, including real-time, data-driven display objects. Users can define context-sensitive help ...

Keywords: graphical user interfaces, prototyping, user interface development tools

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Rigorous Design and Analysis of Behaviour Based Controllers - Martin Westhead (Correct)
and it is not clear that current methodologies and **tools** will be up to the task. There are at least two systems could eventually rival complexity of modern **VLSI** chip designs. In order to make the construction of In the case of behaviour based robots, as with **VLSI** chip design, it is the complexity, or at least the
www.dai.ed.ac.uk/students/martinwe/poster.ps.gz

Implementation Of A Parallel Processing.. - Goulard, Mayrand, .. (Correct)
in IRMAD. Generalized Consistency Checking for **Multiple** variables (GCCM)and Sequential Probability Integrated Remote Monitoring and Diagnostic (IRMAD) **tool** draws upon three domains, software engineering,
www.crm.umontreal.ca/~physnum/WEB_OLD/Physnum/../pub/parallel/rt93.ps.Z

Java Multimedia Studio - Fortino (1997) (Correct)
provide local and distributed synchronization of **multiple** media provide navigation within sessions by In this direction Java Multimedia Studio, a **tool** completely java-based allowing to edit, record
ftp.icsi.berkeley.edu/pub/techreports/1997/tr-97-043.ps.gz

Proving Java Type Soundness - Syme (1997) (Correct) (63 citations)
Note how we name facts, and can have **multiple** (disjunctive) goals. The name auto? indicates proofs that are interesting in their own right. **Tools** for Formal Methods: This work is a major case
www.cl.cam.ac.uk/users/drs1004/java.ps

: A Visual Environment for a Coordination Language - Pascal Bouvry (Correct)
And Produces Manifold Source Code Which Runs On **Multiple**-Platforms: Ibm Sp, Hp, Ibm Rs6000, Sun Os, is hampered by the lack of proper programming **tools**. Software engineering **tools** to assist programmers
www.cwi.nl/ftp/manifold/short_coord96.ps.Z

Specification of Graphic Conventions in Methods - Hofstede, Verhoef, Nieuwland, .. (1992) (Correct)
the Third Workshop on the Next Generation of CASE **Tools**, pages 185-215, Manchester, United Kingdom, May
www.icis.qut.edu.au/~arthur/articles/GraphConv.ps.Z

MRI On The Fly: Accelerating MRI Imaging Using LDA.. - Ko, Taylor (Correct)
time of roughly twenty seconds. Furthermore, **multiple** computers could be used to do this operation, so or MRI, is a non-invasive clinical diagnostic **tool**. The speedier alternative, X-ray computed
ftp.cs.dartmouth.edu/TR/TR96-290.ps.Z

Formal Methods to Aid the Evolution of Software - Ward, Bennett (1995) (Correct) (5 citations)
data structures, and use data structures for **multiple** purposes. Section 5 presents results from using Such an approach clearly lends itself to **tool** support, though the central work of designing the
www.dur.ac.uk/~dcs0mpw/martin/papers/evolution-t.ps.gz

Development of an Intelligent Monitoring and Control System for a.. - Afjeh (1995) (Correct) (8 citations)
is the construction of a performance map from **multiple** runs of the three-dimensional component. A of a monitoring and control system. A monitoring **tool** will allow the user to observe the progress of the
ftp.cs.arizona.edu/schooner/papers/anss28-4-95.ps.Z

Xerox Site Report: Four TREC-4 Tracks - Hearst, Pedersen, Pirolli.. (1996) (Correct) (3 citations)
mode. The goal of the interface was to provide **multiple** ways for the users to view retrieval results, in a graphical user interface to two interactive **tools**, Scatter/Gather [6] and Tilebars [11]and asked
parcftp.xerox.com/pub/hearst/trec4.ps.gz

Reconfigurable Processor for a Data-Flow Video Processing System - Acosta (1995) (Correct) (1 citation)

flexible encoding and decoding, support for **multiple** representations, or algorithmic extensibility, architecture and size of the blocks varies from **vendor** to **vendor** but generally consists of a 2-8 moving scenes, and is intended as both a laboratory **tool** and a prototype architecture for future dsmall.www.media.mit.edu/~vmb/papers/acosta.ps

KBST: A Support Tool for Business Modeling in BSDM - Yun-Heh Chen-Burger (Correct)
the selected generic and the user's model. **Multiple** matches are graded according to an evaluation KBST: A Support **Tool** for Business Modeling in BSDM Yun-heh
www.dai.ed.ac.uk/students/jessicac/psfiles/thesis.ps.gz

Advanced Techniques in Reliability Model Representation and.. - Palumbo, Nicol (1992) (Correct)
The reliability model generator (RMG) is a software **tool** that uses as input a graphical objectoriented
www.kari.re.kr/NASA/larc/92/tp3242.ps.Z

Performance Management Tool for Interoperable Environments - Manning (Correct)
single data model, with complex models requiring **multiple** exchanges connected by Probes. Probes control management services are being provided by current **vendors** of middleware. On the whole we found that no Performance Management **Tool** for Interoperable Environments J.A. McCann, K.J.
www.cs.city.ac.uk/~jam/papers/bcs.ps

Generating The Interface Hierarchy Of A Class Library - Arfi, Godin, Mili, Mineau, .. (Correct)
by the concept lattice is a complex graph with **multiple** sharing of partial interfaces. This is due to Qu'ebec Canada, H3C 3P8 Canada, G1K 7P4 ABSTRACT A **tool** for generating the interface hierarchy of a set of
www.info.uqam.ca/~missaoui/Papers/ToWorld.ps

The "Petri Net Baukasten": An Overview - Gajewsky, Ehrig (2001) (Correct)
Common Base is an acylic directed graph, because **multiple** inheritance is allowed. The root of our Petri with dierent views on theory, application, and **tools** of Petri nets: The Expert View, the Application
user.cs.tu-berlin.de/~magda/Papers/unifyPN.ps.gz

A Modular Framework for the Integration of Heterogeneous.. - Büssow, Grieskamp (Correct)
for the Integration of Heterogeneous Notations and **Tools** Robert Bussow and Wolfgang Grieskamp Technische
uebb.cs.tu-berlin.de/~wg/papers/ModularFramework.ps.gz

Efficient Scene Descriptions Using Advanced Modelling.. - Schultz, Schumann (2000) (Correct)
and cannot be achieved in practice because of **multiple** overheads that result e.g. from the size of the instancing (referencing) procedural objects, and **tool** objects are discussed. We introduce the concepts
www.icg.informatik.uni-rostock.de/~schumann/papers/schultz.pdf

An International Survey of Industrial Applications of.. - Craigen, Gerhart.. (1993) (Correct) (57 citations)
channels, neutronic parameters are measured by **multiple** in-core flux detectors and one ion chamber. prototype in the field in order to drive smartcard **vendors**. 8.4.3 Process features General process effects techniques, often supported by reasoning **tools**, that can offer a rigorous and effective way to
ftp.ora.on.ca/pub/doc/93-626-v2.ps.Z

Participatory Adaptation - Rozier, Alterman (1997) (Correct)
our data. The MULTICASE is a method for merging **multiple** episodes of routine activity into a single knowledge is important for working with a computer **tool** effectively. Expert users of particular computer
www.cs.brandeis.edu/~sklar/chi97.ps

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... CPLDs, the epitome of **VLSI**, integrate so much and such ... and its corresponding development-**tool** set One board's tools ...
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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Evaluation of vendor products: CASE tools in support of work groups**
Vessey, I.; Sravanapudi, A.;
System Sciences, 1992. Proceedings of the Twenty-Fifth Hawaii International Conference on , Volume: iv , 7-10 Jan. 1992
Pages:420 - 431 vol.4

[Abstract] [PDF Full-Text (952 KB)] **IEEE CNF**

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2 **Emerging standards for component software**
Adler, R.M.;
Computer , Volume: 28 , Issue: 3 , March 1995
Pages:68 - 77

[Abstract] [PDF Full-Text (1056 KB)] **IEEE JNL**

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